ABSTRACT OF THE DISCLOSURE

The invention provides a method of analyzing a source current at a higher speed and an enhanced accuracy in a semiconductor integrated circuit including a digital circuit. The method to analyze a waveform of the source current, with consideration of re-distribution of charges throughout the digital circuit in the semiconductor integrated circuit, expressing the digital circuit with series of parasitic capacitors $\Sigma C_{ch,\uparrow}(nT)$ and $\Sigma C_{ch,\downarrow}(nT)$ to be charged and connected between the source and the ground lines. The capacitor series are calculated in time series based on the distribution of switching operations of the logic gates included in the digital circuit. An analysis model for determining the waveform of the source current in the digital circuit is obtained by connecting the parasitic capacitor series with a couple of respective parasitic impedances Z_d and Z_g of the source line and the ground line.